Application No.: 09/926,791

Art Unit: 2818

Examiner: Michael T. TRAN

LIST OF CURRENT CLAIMS

1. (Currently amended) A semiconductor memory chip module comprising a first memory chip (4) of a first type, a second memory chip (6) of a second type <u>different from the first type of memory chip</u>, and an electric connection (14, 16) between the first and second memory chips (4, 6), wherein the memory chips (4, 6) are disposed one above the other in different levels and connected by vertical chip interconnections (14, 16).

- 2. (Previously amended) A chip module according to claim 1, wherein memory cells (C4) of the first memory chip (4) are firmly allocated to certain memory cells (C6) of the second memory chip (6), and the mutually allocated memory cells (C4, C6) are directly interconnected electrically.
- 3. (Previously amended) A chip module according to claim 1, wherein the first type corresponds to a nonvolatile memory, for example EEPROM, and the second type to a volatile memory, for example SRAM.
- 4. (Previously amended) A chip module according to claim 1, wherein at least one further chip (8, 16) is provided in a further level.
- 5. (Previously amended) A chip module according to claim 4, wherein the further chip contains decoder circuits (10, 12) for the memory chips (4, 6).
- 6. (Previously amended) A chip module according to claim 1, wherein an energy buffer is formed in at least one of the levels.
- 7. (Previously amended) A chip module according to claim 6, wherein the energy buffer is formed as an integrated buffer capacitor (20).
- 8. (Previously amended) A chip module according to claim 1, formed for a smart card.



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9. (Previously amended) A smart card having a semiconductor memory chip module according to claim 1.